The City School

Mid-Year Examinations
2016-17
Class 10

CANDIDATE NAME:

INDEX NUMBER:

DATE: _____

COMPUTER SCIENCE **2210/01**

Candidates answer on the Question Paper. 1 Hour 45 minutes

No Additional Materials are required.

READ THESE INSTRUCTIONS FIRST

Write your name, index number and date on all the work you hand in.
Write in dark blue or black pen on both sides of the paper.
Do not use staples, paper clips, highlighters, glue or correction fluid.
Calculators must not be used in this paper.

Answer **ALL** questions.

At the end of the examination, fasten all your work securely together.
The number of marks is given in brackets [ ] at the end of each question or part question.
The maximum number of marks is 75.

This document consists of 13 printed pages

1. Name four types of logic gate, draw their symbols and complete their associated truth tables:

Gate 1: _____

Symbol:

A	B	X
0	0	
0	1	
1	0	
1	1	

Gate 2: _____

Symbol:

A	B	X
0	0	
0	1	
1	0	
1	1	

Gate 3: _____

Symbol:

A	B	X
0	0	
0	1	
1	0	
1	1	

Gate 4: _____

Symbol:

A	B	X
0	0	
0	1	
1	0	
1	1	

[8]

2. A computer-controlled machine produces plastic sheets. The thickness of each sheet must be within a certain tolerance. The sheets are kept below 50 °C as they move over rollers at 10 metres per second.

Three parameters need to be monitored all the time.

Parameter	Description	Binary value	Conditions
D	sheet thickness	1	thickness of sheet in tolerance
		0	thickness of sheet out of tolerance
S	roller speed	1	roller speed = 10 metres/second
		0	roller speed <> 10 metres/second
T	temperature	1	temperature < 50°C
		0	temperature >= 50°C

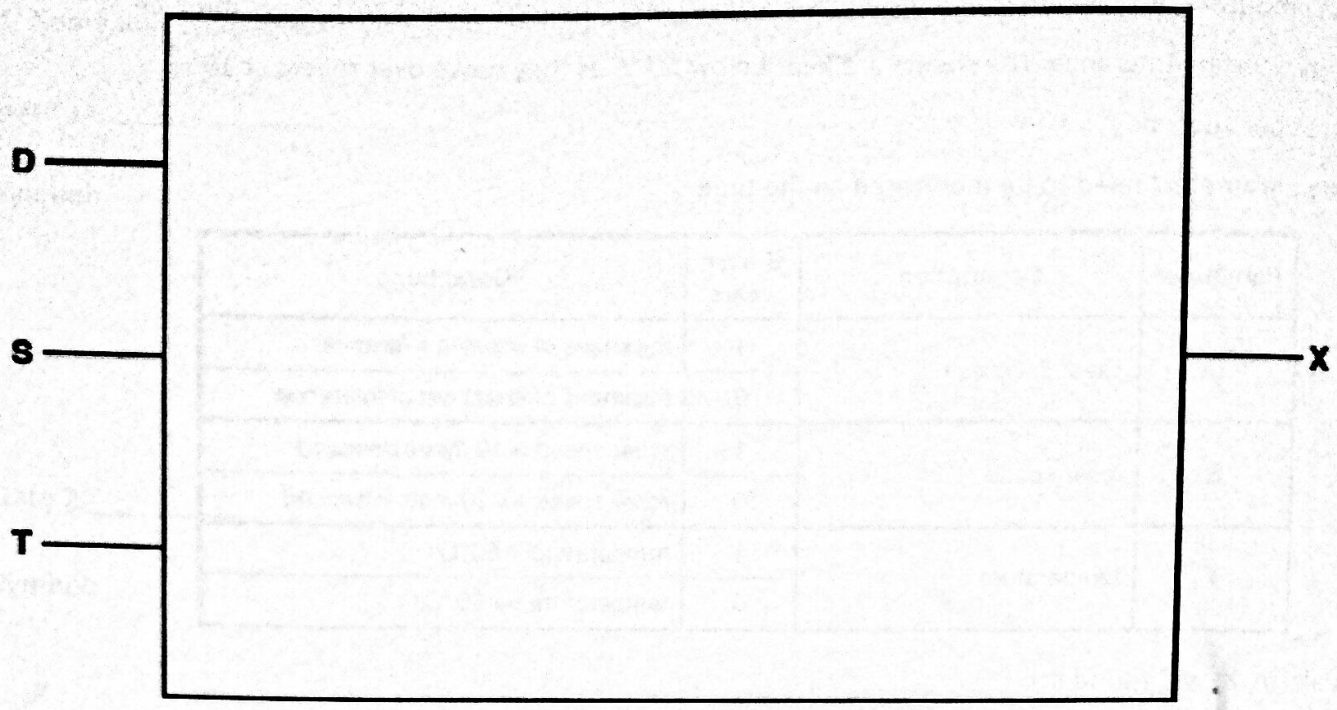
An alarm, **X**, will sound if:

thickness is in tolerance AND (roller speed <> 10 metres/second OR temperature >= 50 °C)

OR

roller speed = 10 metres/second AND temperature >= 50 °C

(a) Draw a logic circuit to represent the above monitoring system.



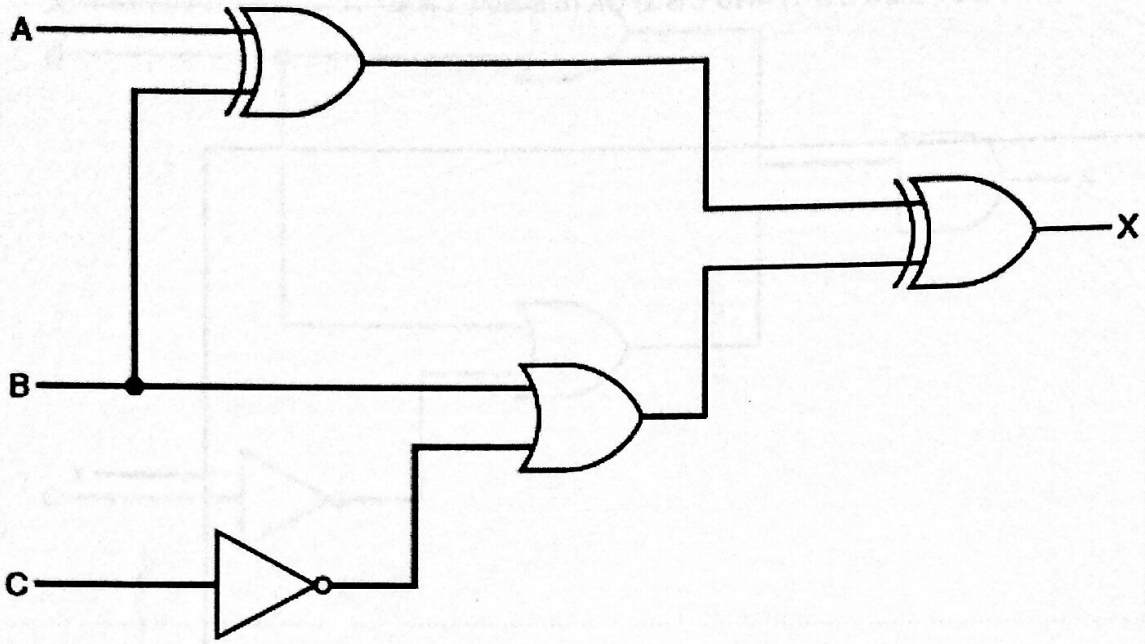
[6]

(b) Complete the truth table for the monitoring system.

D	S	T	Working Space	X
0	0	0		
0	0	1		
0	1	0		
0	1	1		
1	0	0		
1	0	1		
1	1	0		
1	1	1		

[8]

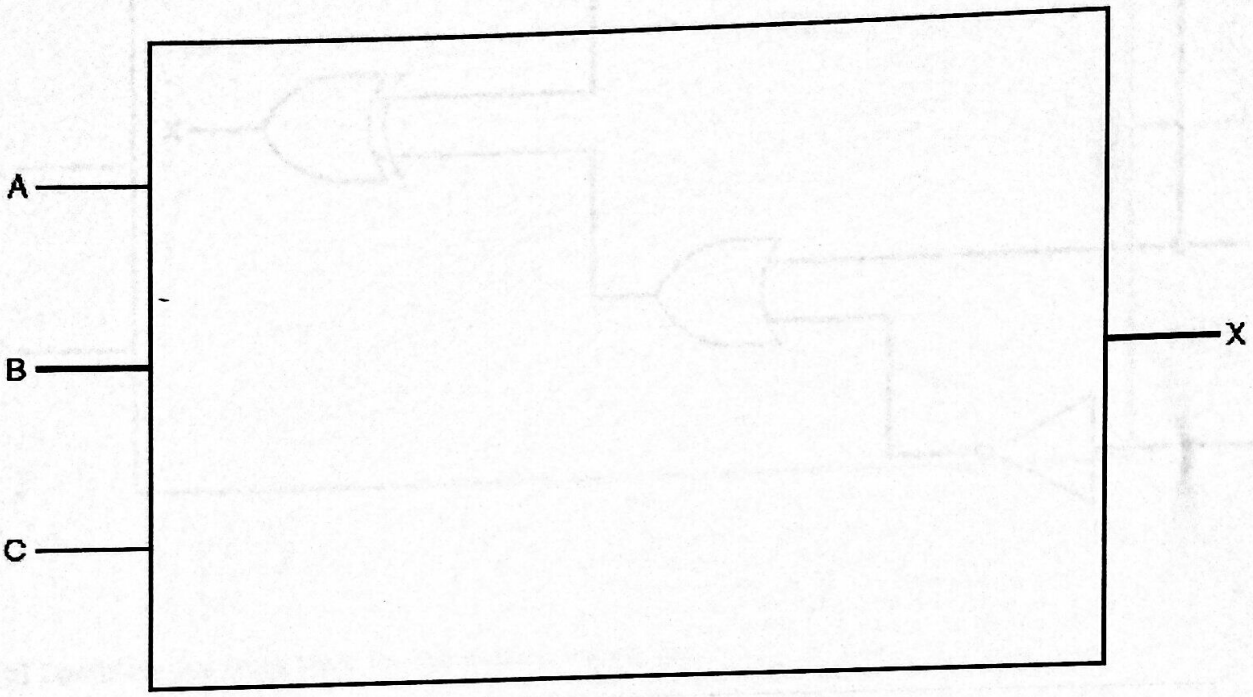
3 (a) Complete the truth table for the following logic circuit:



A	B	C	Working Space	X
0	0	0		
0	0	1		
0	1	0		
0	1	1		
1	0	0		
1	0	1		
1	1	0		
1	1	1		

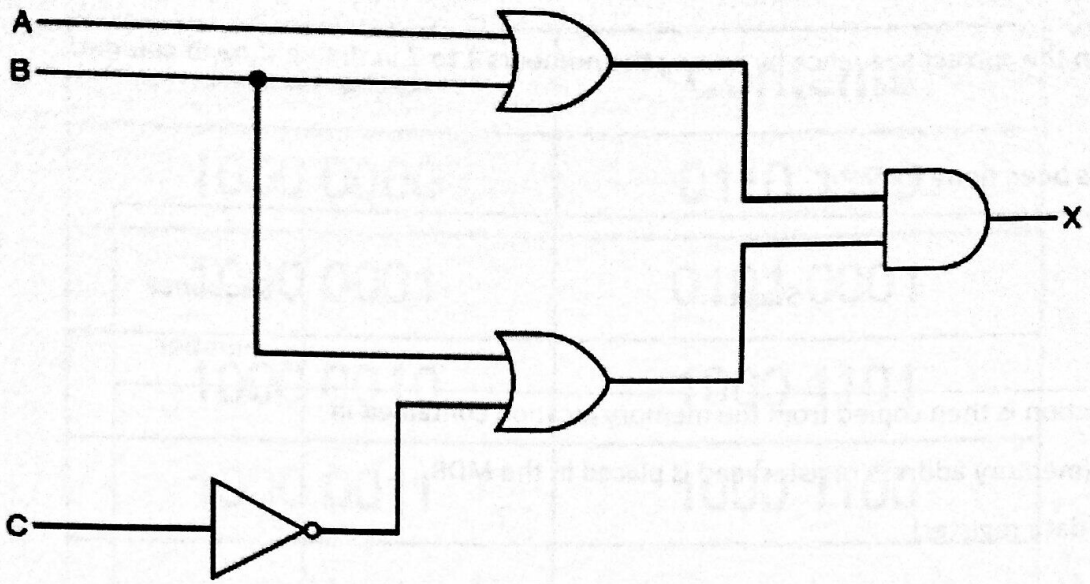
[8]

(b) Draw a logic circuit which corresponds to the following logic statement: X = 1 if ((A is **NOT** 1 **OR** B is 1) **AND** C is 1) **OR** (B is **NOT** 1 **AND** C is 1)



[6]

(c) Write a logic statement which corresponds to the following logic circuit:



.....

..... [4]

4 (a) One of the key features of von Neumann computer architecture is the use of buses. Three buses and three descriptions are shown below.

Draw a line to connect each bus to its correct description.

Bus	Description
address bus	this bus carries signals used to coordinate the computer's activities
control bus	this bi-directional bus is used to exchange data between processor, memory and input/ output devices
data bus	this uni-directional bus carries signals relating to memory addresses between processor and memory

[3]

(b) The seven stages in a von Neumann fetch-execute cycle are shown in the table below.

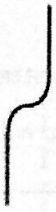
Put each stage in the correct sequence by writing the numbers 1 to 7 in the right hand column.

The first one has been done for you.

Stage	Sequence number
the instruction is then copied from the memory location contained in the MAR (memory address register) and is placed in the MDR (memory data register) be fetched	
the instruction is finally decoded and is then executed	
the PC (program counter) contains the address of the next instruction to be fetched	1
the entire instruction is then copied from the MDR (memory data register) and placed in the CIR (current instruction register)	
the address contained in the PC (program counter) is copied to the MAR (memory address register) via the address bus	
the address part of the instruction, if any, is placed in the MAR (memory address register)	
the value in the PC (program counter) is then incremented so that it points to the next instruction ~~to~~	

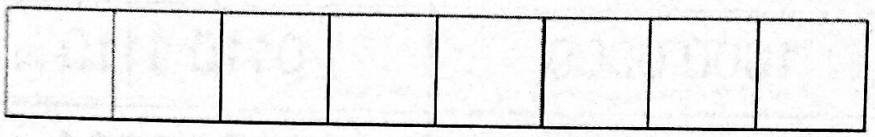
[6]

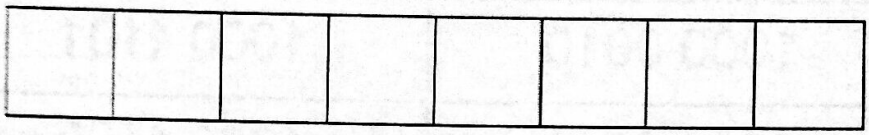
5. A section of computer memory is shown below:

Address	Contents
1000 0000	0110 1110
1000 0001	0101 0001
1000 0010	1000 1101
1000 0011	1000 1100
	
1000 1100	
1000 1101	
1000 1110	
1000 1111	

(a) (i) The contents of memory location 1000 0001 are to be read.

Show the contents of the Memory Address Register (MAR) and the Memory Data Register (MDR) during this read operation:

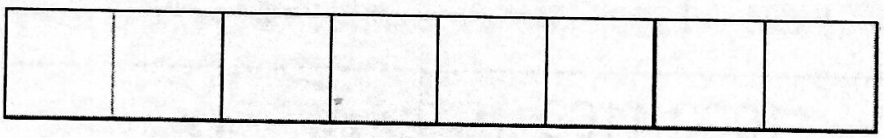
MAR 

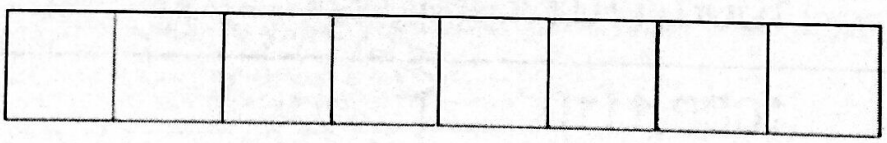
MDR 

[2]

(ii) The value 0111 1001 is to be written into memory location 1000 1110.

Show the contents of the MAR and MDR during this write operation:

MAR 

MDR 

[2]

(iii) Show any changes to the computer memory following the read and write operations in **part (a)(i)** and **part (a)(ii)**.

Address	Contents
1000 0000	0110 1110
1000 0001	0101 0001
1000 0010	1000 1101
1000 0011	1000 1100
1000 1100	
1000 1101	
1000 1110	
1000 1111	

[2]

(b) Name **three** other registers used in computers.

1 .....

2 .....

3 ..... **[3]**

(c) The control unit is part of a computer system.

What is the function of the control unit?

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.....

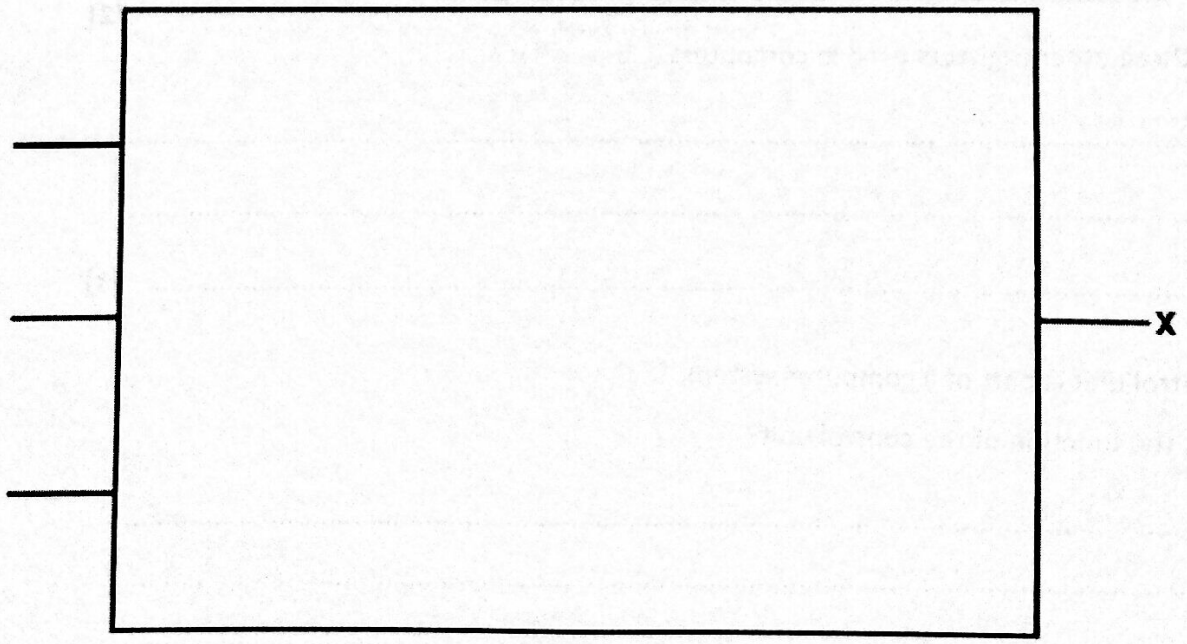
..... **[3]**

6. A manufacturing process is controlled by a built in logic circuit which is made up of AND, OR and NOT gates only. The process receives a STOP signal
(i.e. X = 1) depending on certain conditions, shown in the following table:

INPUTS	BINARY VALUES	CONDITION IN PROCESS
V	1	Volume > 1000 litres
	0	Volume <= 1000 litres
T	1	Temperature > 750ºC
	0	Temperature <= 750ºC
S	1	Speed > 15 metres/second (m/s)
	0	Speed <= 15 metres/ second (m/s)

A stop signal (X = 1) occurs when:
either Volume, V > 1000 litres and Speed, S <= 15 m/s or
Temperature, T <= 750ºC and Speed, S > 15 m/s

(a) Draw the logic circuit and truth table to show all the possible situations when the stop signal could be received.



[6]

(b) Complete the truth table for the above logic circuit

INPUT V	INPUT T	INPUT S	OUTPUT X
0	0	0	
0	0	1	
0	1	0	
0	1	1	
1	0	0	
1	0	1	
1	1	0	
1	1	1	

[8]